AN2834
Application note

How to get the best ADC accuracy in STM32F10xxx devices

Introduction

The STM32F10xxx microcontroller family embeds up to three advanced 12-bit ADCs (depending on the device) with a conversion time down to 1 µs. A self-calibration feature is provided to enhance ADC accuracy versus environmental condition changes.

In applications involving analog-to-digital conversion, ADC accuracy has an impact on the overall system quality and efficiency. To improve this accuracy, you need to understand the errors associated with the ADC and the parameters affecting them.

The ADC accuracy cannot depend on the ADC performance and features only, it depends on the overall application design around the ADC.

The aim of this application note is to help understand ADC errors and how to enhance ADC accuracy. The document is divided into two main parts:

- in the first, it gives the different types and sources of ADC errors related to the ADC design and to external ADC parameters such as the external hardware design
- in the second part, it describes the different recommendations and gives hints on how to minimize these errors by focusing on the hardware methods

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1 Different ADC errors

1.1 ADC errors related to the ADC itself

Different accuracy error types are specified for the STM32F10xxx ADC. Accuracy errors are normally expressed as multiples of 1 LSB for easy reference. The resolution in terms of voltage depends on the reference voltage. The error in terms of voltage is calculated by multiplying the number of LSBs with the voltage corresponding to 1LSB (1LSB = $V_{REF+}/2^{12}$ or $V_{DDA}/2^{12}$).

1.1.1 Offset error

It is defined as the deviation between the first actual transition and the first ideal transition. The first transition occurs when the digital output of the ADC changes from 0 to 1. Ideally, when the analog input is between 0.5 LSB and 1.5LSB, the digital output should be 1. Ideally still, the first transition occurs at 0.5 LSB. The offset error is denoted by E_O.

Example

For the STM32F10xxx ADC, the smallest detectable incremental change in voltage is expressed in terms of LSBs:

1 LSB = $V_{REF+}/4096$ (or $V_{DDA}/4096$ depending on the package).

If V_{REF+} = 3.3 V, ideally, the input of 402.8 µV (0.5 LSB = 0.5 × 805.6 µV) should lead to the generation of a digital output of 1. In practice, however, the ADC may still show the reading as 0. If a digital output of 1 is obtained from an analog input of 550 µV, then:

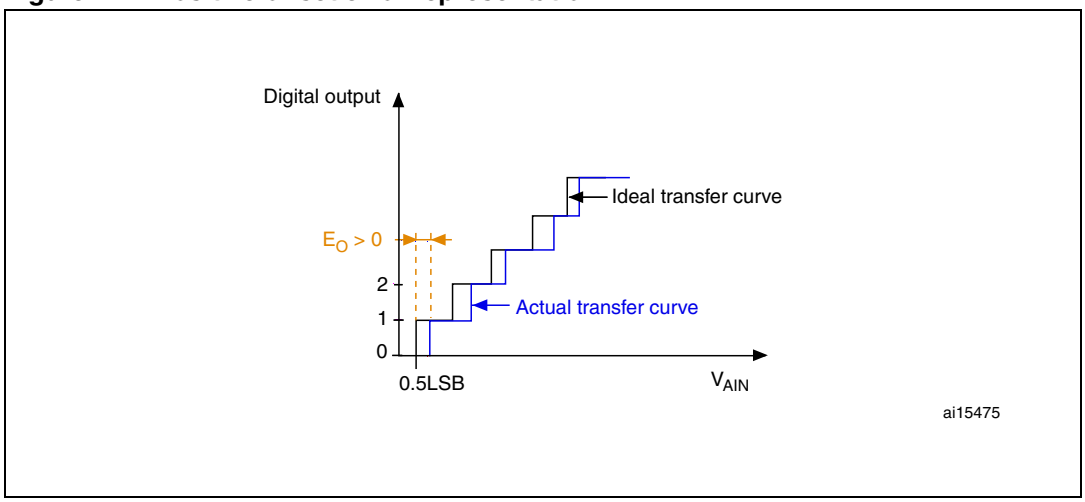
Offset error = Actual transition – Ideal transition

E_O = 550 µV – 402.8 µV = 141.2 µV

E_O = 141.2 µV / 805.6 µV = 0.17 LSB

When an analog input voltage greater than 0.5LSB generates the first transition, the offset error is positive. *Figure 1* shows a positive offset error.

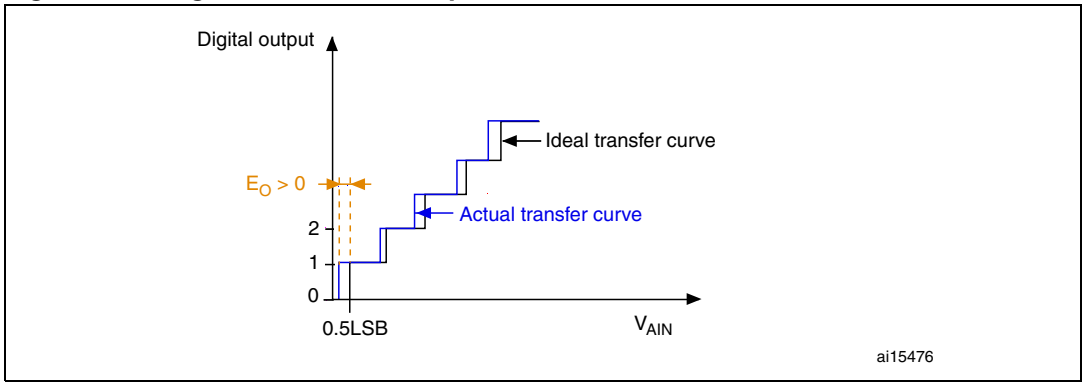
Figure 1. Positive offset error representation



When an analog input voltage of less than 0.5LSB generates the first transition, the offset error is negative. *Figure 2* shows a negative offset error.

If the analog input voltage $V_{AIN} = V_{SSA}$ and the ADC generates a nonzero digital output, the offset error is negative. This means that a negative voltage generates the first transition.

Figure 2. Negative offset error representation



1.1.2 Gain error

Gain error is defined as the deviation between the last actual transition and the last ideal transition. Gain error is represented as E_G.

The last actual transition is the transition from FFEh to FFFh. Ideally, there should be a transition from FFEh to FFFh, when the analog input is equal to $V_{REF+} – 0.5LSB$. So for V_{REF+}= 3.3 V, the last ideal transition should be at 3.299597 V.

If the ADC provides the FFFh reading for $V_{AIN} < V_{REF+} – 0.5LSB$, then we have a negative gain error.

Example

Gain error E_G = Last actual transition – ideal transition

If V_{REF+} = 3.3 V and V_{AIN} = 3.298435 V generates a transition from FFE to FFF then,

E_G = 3.298435 V – 3.299597 V

E_G = –1162 µV

E_G = (–1162 µV / 805.6 µV) LSB = –1.44 LSB

If we do not get a full scale reading (FFFh) for V_{AIN} equal to V_{REF+}, the gain error is positive. This means that a voltage greater than V_{REF+} will cause the last transition. *Figure 3* shows a positive gain error and *Figure 4*, a negative gain error.

Figure 3. Positive gain error representation

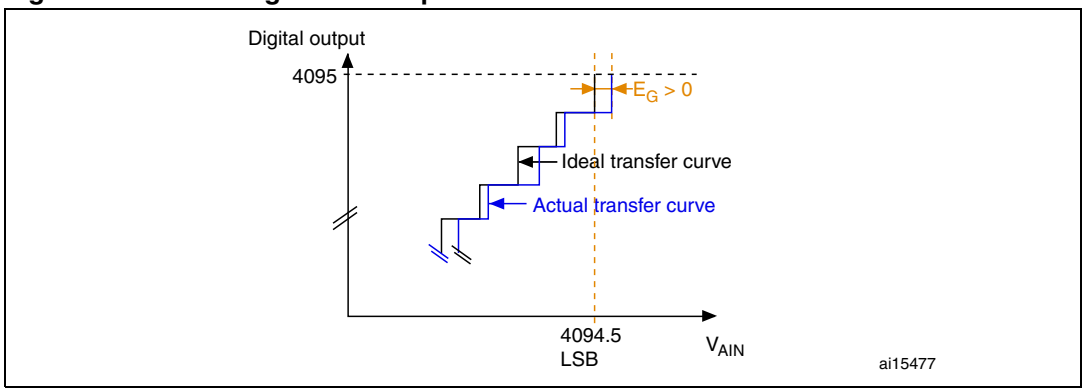
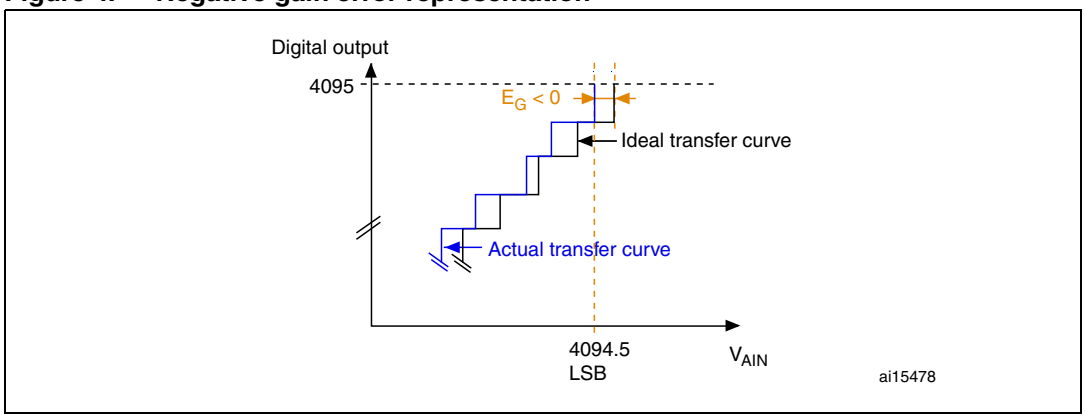


Figure 4. Negative gain error representation



1.1.3 Differential linearity error

The differential linearity error (DLE) is defined as the maximum deviation between the actual and ideal steps. Here 'ideal' is not used for the ideal transfer curve but for the resolution of the ADC. The DLE is denoted by E_D. It is represented in *Figure 5*.

E_D = Actual step width – 1LSB

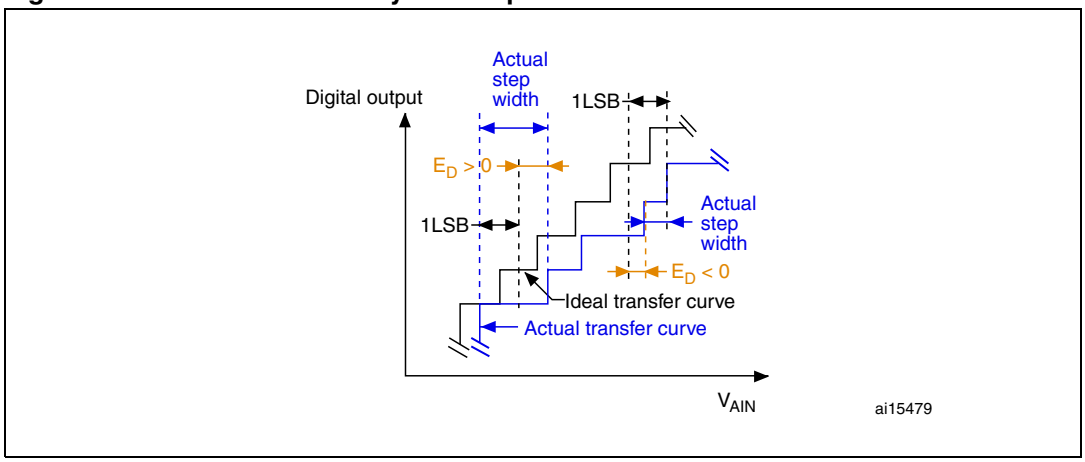
Ideally, an analog input voltage change of 1LSB should cause a change in the digital code. If an analog input voltage greater than 1LSB is required for a change in digital code, the ADC has a differential linearity error. The DLE therefore corresponds to the maximum additional voltage that is required to change from one digital code to the next.

The DLE is also known as the differential non-linearity (DNL) error.

Example

A given digital output should correspond to an analog input range. Ideally, the step width should be 1LSB. Let us assume that we get the same digital output over an analog input voltage range of 1.9998 V to 2.0014 V, the step width will be 2.0014 V – 1.9998 V = 1.6 mV. E_D is thus the voltage difference between the higher (2.0014 V) and lower (1.9998 V) analog voltages less the voltage corresponding to 1LSB.

Figure 5. Differential linearity error representation



If V_{REF+} = 3.3 V, an analog input of 1.9998 V (9B1h) can provide results varying between 9B0h and 9B2h. Similarly, for an input of 2.0014 V (9B3h), the results may vary between 9B2h and 9B4h.
Thus, the total voltage variation corresponding to the 9B2h step is:

9B3h – 9B1h, that is, 2.0014 V – 1.9998V = 1.6 mV (1660 µV)

E_D= 1660 µV – 805.6 µV

E_D= 854.4 µV

E_D= (854.4 µV/805.6 µV) LSB

E_D= 1.06 LSB

Let us assume that no voltage greater than 2.0014 V will result in the 9B2h digital code. When the step width is less than 1LSB, E_D is negative.

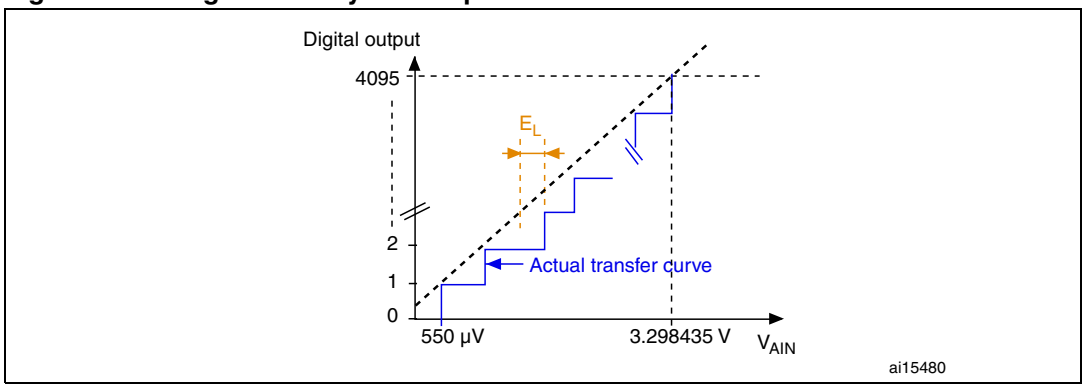
1.1.4 Integral linearity error

The integral linearity error is the maximum deviation between any actual transition and the endpoint correlation line. The ILE is denoted by E_L. It is represented in *Figure 6*.

The endpoint correlation line can be defined as the line on the A/D transfer curve that connects the first actual transition with the last actual transition. E_L is the deviation from this line for each transition. The endpoint correlation line thus corresponds to the actual transfer curve and has no relation to the ideal transfer curve.

The ILE is also known as the integral non linearity error (INL). The ILE is the integral of the DLE over the whole range.

Figure 6. Integral linearity error representation



Example

If the first transition from 0 to 1 occurs at 550 µV and the last transition (FFEh to FFFh) occurs at 3.298435 V (gain error), then the line on the transfer curve connecting the actual digital codes 1h and FFFh will be the endpoint correlation line.

1.1.5 Total unadjusted error

the total unadjusted error (TUE) is defined as the maximum deviation between the actual and the ideal transfer curves. It is a parameter that specifies the total errors that may occur, causing maximum deviation between the ideal digital output and the actual digital output. It is the maximum deviation recorded between the ideal expected value and the actual value obtained from the ADC for any input voltage. The TUE is denoted by E_T. It is represented in *Figure 7*.

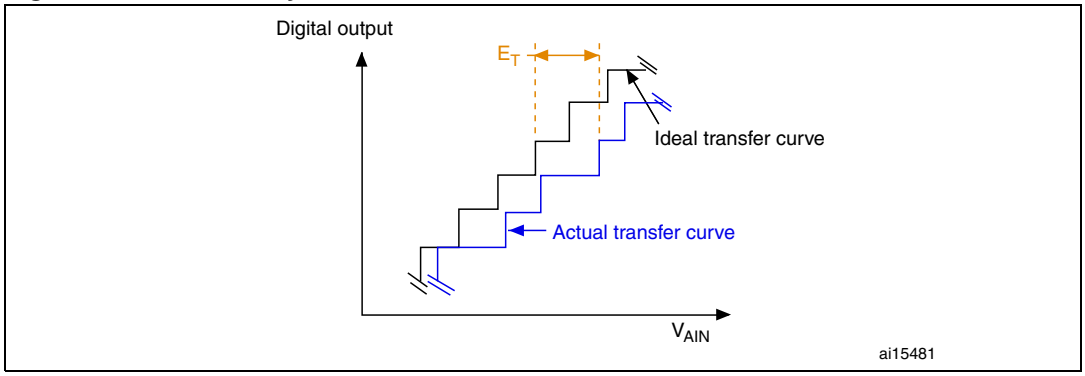
The TUE is not the sum of E_O, E_G, E_L, E_D. The offset error affects the digital result at lower voltages whereas the gain error affects the digital output for higher voltages.

Example

If V_{REF+} = 3.3 V and V_{AIN} = 2 V, the ideal result is 9B2h. But if, on conversion, we get the result 9B4h, the deviation may result from the offset since the DLE and ILE errors occur simultaneously.

TUE = absolute (actual value – ideal case value) = 9B4h – 9B2h = 2h = 2LSB

Figure 7. Total unadjusted error



1.2 ADC errors related to its environment

1.2.1 Power supply noise

The analog power supply is used as the reference voltage for conversion. As the ADC output is the ratio between the analog signal voltage and the supply voltage, any noise on the analog reference will cause a change in the converted digital value.

For example, with an analog reference of 3.3 V and a 1 V signal input, the converted result is (1/3.3) × 4095 = 4D9h

But with a 40 mV peak-to-peak ripple in the power supply, the converted value becomes (1/3.34) × 4095 = 4CAh (with V_{REF+} at its peak).

Error = 4D9 – 4CA = 15 LSB

The SMPS (switch-mode power supply) normally has internal fast-switching power transistors. This introduces high-frequency noise in the output. The switching noise is in the range of 15 kHz to 1 MHz.

1.2.2 Power supply regulation

Power supply regulation is very important for ADC accuracy since the conversion result is the ratio of the analog input voltage to the V_{REF+} value.

If the power supply output decreases when connected to V_{DDA} or V_{REF+} due to the loads on these inputs and to its output impedance, an error will be introduced in the conversion result.

$\text{Digital}_{output} = \frac{V_{AIN}(2^n - 1)}{V_{REF+}}$, where n is the resolution of the ADC (in our case n = 12).

If the reference voltage changes, the digital result changes too.

For example:

If the supply used is a reference voltage of 3.3 V and V_{AIN} = 1 V, the digital output is:

$$\text{Digital}_{output} = \frac{1 \times (2^{12} - 1)}{3.3} = 4D9h$$

If the voltage supply provides a voltage equal to 3.292 V (after its output connection to V_{REF+}), then:

$$\text{Digital}_{output} = \frac{1 \times (2^{12} - 1)}{3.292} = 4DCh$$

The error introduced by the voltage drop is: 4DC – 4D9 = 3LSB

1.2.3 Analog input signal noise

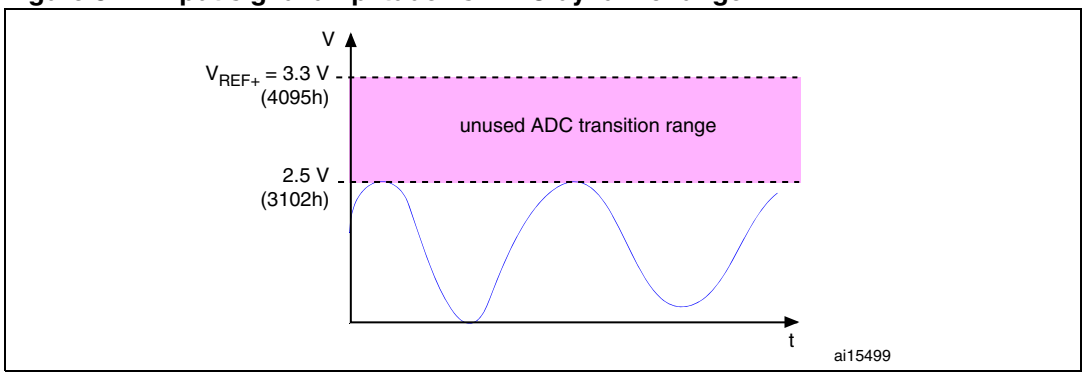
Small but high-frequency signal variation can result in big conversion errors during sampling time. This noise is generated by electrical devices, for example, motors, engine ignition, power lines, and so on, and affects the source signal (for example a sensor) by adding an unwanted signal. As a consequence, the conversion results of the ADC are not accurate.

1.2.4 ADC dynamic range badly matching the maximum input signal amplitude

It is very important that the ADC dynamic range matches the maximum amplitude of the signal to be converted to have the maximum ADC conversion precision. Let us assume that the signal to be converted varies between 0 V to 2.5 V and that V_{REF+} is equal to 3.3 V. The maximum signal value converted by the ADC is 3102 (2.5 V) as shown in *Figure 8*. In this case, there are 993 unused transitions (4095 – 3102 = 993). This implies a loss in the converted signal accuracy.

See *Section 2.2.4: Matching the ADC dynamic range to the maximum signal amplitude on page 17* for details on how to have the ADC dynamic range matching the maximum input signal amplitude.

Figure 8. Input signal amplitude vs. ADC dynamic range



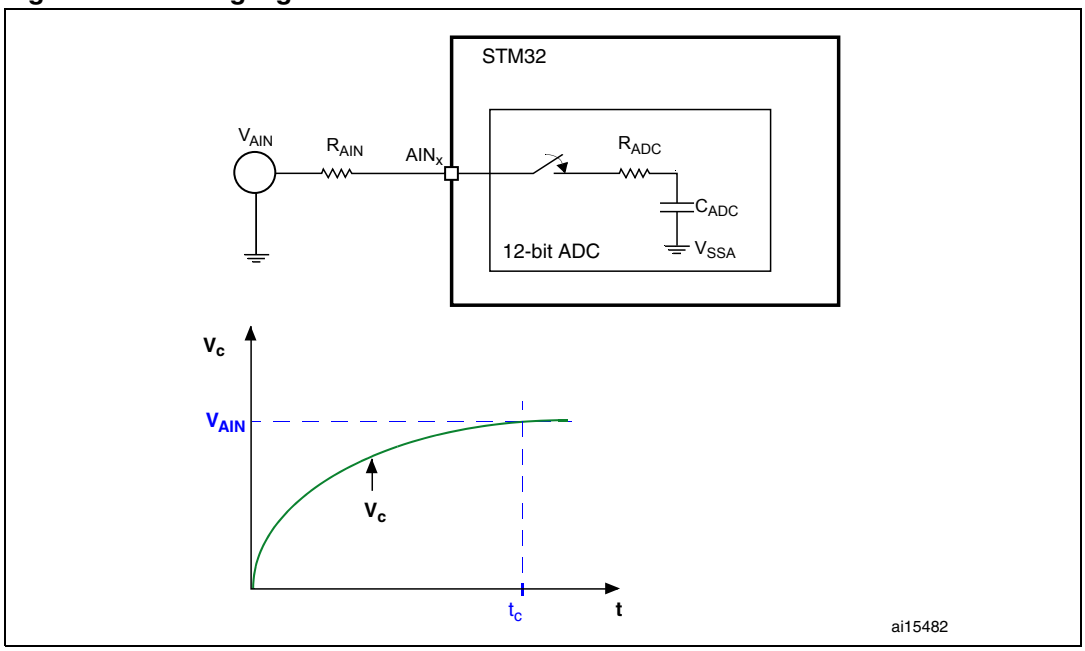
1.2.5 Effect of the analog signal source resistance

The impedance of the analog signal source, or series resistance (R_{AIN}), between the source and pin causes a voltage drop across it because of the current flowing into the pin. Together R_{ADC} and C_{ADC} form an RC network. The charging of the capacitor is controlled by R_{ADC}.

With the addition of source resistance (with R_{ADC}), the time required to fully charge the hold capacitor increases. *Figure 9* shows the analog signal source resistance effect.

The effective charging of C_{ADC} is governed by $R_{ADC} + R_{AIN}$, so the charging time constant becomes $t_c = (R_{ADC}+R_{AIN}) \times C_{ADC}$. If the sampling time is less than the time required to fully charge the C_{ADC} through $R_{ADC} + R_{AIN}$ ($t_s < t_c$), the digital value converted by the ADC is less than the actual value.

Figure 9. Analog signal source resistance effect



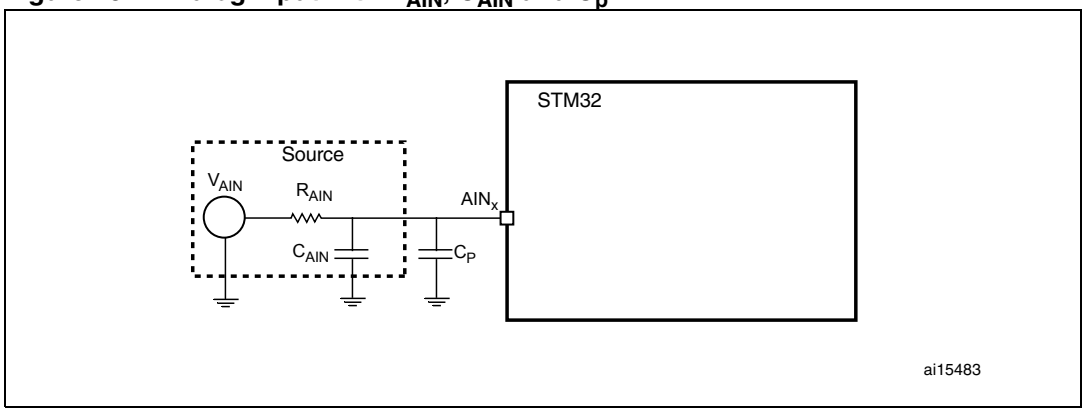
1. t_c is the time taken by the C_{ADC} capacitor to fully charge: $V_c = V_{AIN}$
   V_c: capacitor (C_{ADC}) voltage
   $t_c = (R_{ADC} + R_{AIN}) \times C_{ADC}$

1.2.6 Effect of the source capacitance and parasitic capacitance of the PCB

When converting analog signals, it is necessary to account for the capacitance at the source and the parasitic capacitance seen on the analog input pin (refer to *Figure 10*). The source resistance and capacitance form an RC network and the ADC conversion results may not be accurate unless the external capacitor ($C_{AIN} + C_p$) is fully charged to the level of the input voltage. The greater value of ($C_{AIN} + C_p$), the more limited the source frequency.

The external capacitance at the source and the parasitic capacitance are denoted by C_{AIN} and C_p, respectively.

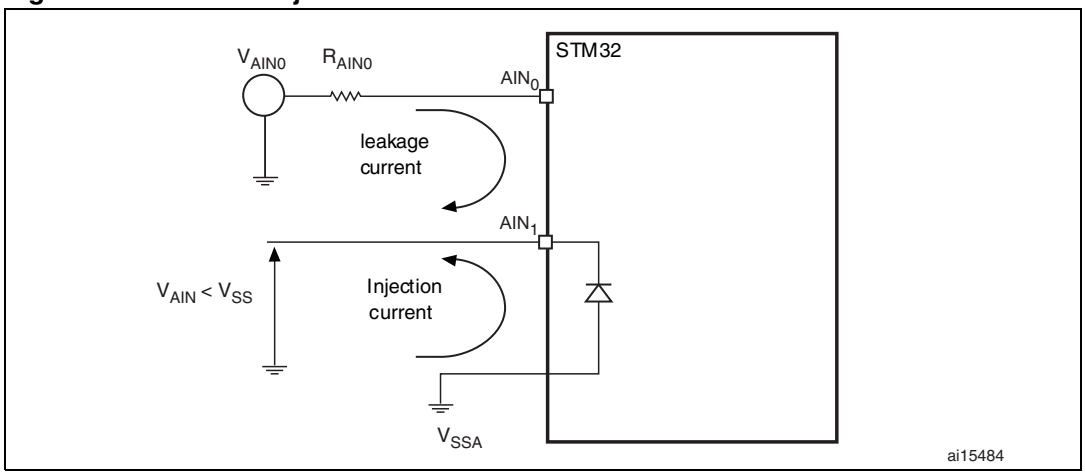
Figure 10. Analog input with R_{AIN}, C_{AIN} and C_p



1.2.7 Injection current effect

A negative injection current on any analog pin (or a closely positioned digital input pin) may introduce leakage current into the ADC input. The worst case is the adjacent analog channel. A negative injection current is introduced when $V_{AIN} < V_{SS}$, causing current to flow out from the I/O pin. This is illustrated in *Figure 11*.

Figure 11. Effect of injection current



1.2.8 Temperature influence

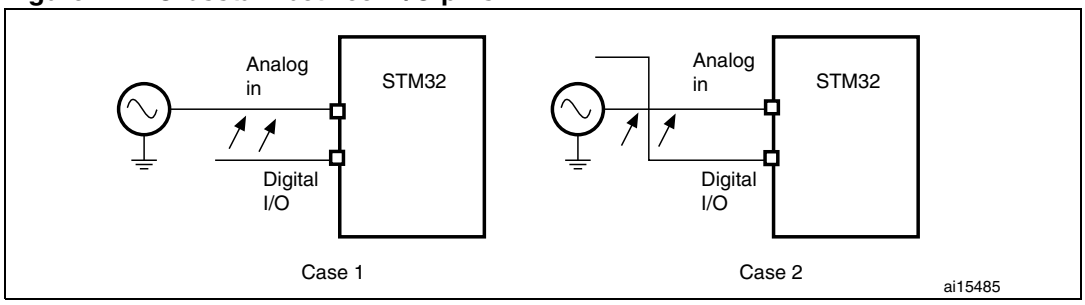
The temperature has a major influence on ADC accuracy. Mainly it leads to two major errors: offset error and gain error. Those errors can be compensated in the microcontroller firmware (refer to *Section 2.2.7* for the temperature-compensation methods).

1.2.9 I/O pin crosstalk

Switching the I/Os may induce some noise in the analog input of the ADC due to capacitive coupling between I/Os. Crosstalk may be introduced by PCB tracks that run close to each other or that cross each other.

Internally switching digital signals and I/Os introduces high-frequency noise. Switching high-sink I/Os may induce some voltage dips in the power supply caused by current surges. A digital track that crosses an analog input track on the PCB may affect the analog signal (see *Figure 12*).

Figure 12. Crosstalk between I/O pins



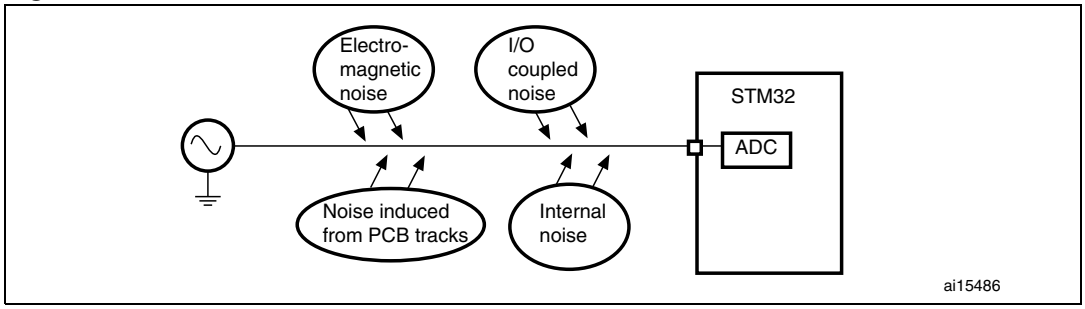
Case 1: Digital and analog signal tracks that pass close to each other.

Case 2: Digital and analog signal tracks that cross each other on a different PCB side.

1.2.10 EMI-induced noise

Electromagnetic emissions from neighboring circuits may introduce high-frequency noise in an analog signal because the PCB tracks may act like an antenna (See *Figure 13.*).

Figure 13. EMI sources



2 How to get the best ADC accuracy

2.1 Recommendation to reduce the effects of ADC-related ADC errors

The TUE is not the sum of all the errors E_O, E_G, E_L, E_D. It is the maximum deviation that can occur between the ideal and actual digital values. It can result from one or more errors occurring simultaneously.

As the ILE is the integral of the DLE, it can be considered as the indicator of the maximum error. Do not add the DLE and ILE together to calculate the maximum error that may occur at any digital step.

The ILE and DLE are dependent on the ADC design. It is difficult to calibrate them. They can be minimized by doing multiple conversions and then averaging.

Offset and gain errors can be easily compensated using the STM32F10xxx ADC self-calibration feature.

The maximum error values specified in the datasheet are the worst error values measured in laboratory test environment over the full voltage range.

2.2 How to minimize ADC errors related to the external environment of the ADC

2.2.1 Power-supply noise minimization

Power supply side

Linear regulators have a better output in terms of noise. The mains must be stepped down, rectified and filtered, then fed to linear regulators. It is highly recommended to connect the filter capacitors to the rectifier output. Please refer to the datasheet of the used linear regulator.

If you are using a switching power supply, it is recommended to have a linear regulator to supply the analog stage.

It is recommended to connect capacitors with good high-frequency characteristics between the power and ground lines. That is, a 0.1 µF and a 1 to 10 µF capacitor should be placed close to the power source.

The capacitors allow the AC signals to pass through them. The small-value capacitors filter high-frequency noise and the high-value capacitors filter low-frequency noise. Ceramic capacitors are generally available in small values (1 pF to 0.1 µF) and with small voltage ratings (16 V to 50 V). It is recommended to place them close to the main supply (V_{DD} and V_{SS}) and analog supply (V_{DDA} and V_{SSA}) pins. They filter the noise induced in the PCB tracks. Small capacitors can react fast to current surges and discharge quickly for fast-current requirements.

Tantalum capacitors can also be used along with ceramic capacitors. To filter low-frequency noise, you can use high-value capacitors (10 µF to 100 µF), which are generally electrolytic. It is recommended to put them near the power source.
To filter high-frequency noise, you can use a ferrite inductance in series with the power

supply. This solution leads to very low (negligible) DC loss unless the current is high because the series resistance of the wire is very low. At high frequencies, however, the impedance is high.

STM32F10xxx side

In most STM32F10xxx microcontrollers the V_{DD} and V_{SS} pins are placed close to each other. So are the V_{REF+} and V_{SSA} pins. A capacitor can therefore be connected very close to the microcontroller with very short leads. For multiple V_{DD} and V_{SS} pins, use separate decoupling capacitors.

The V_{DDA} pin must be connected to two external decoupling capacitors (10 nF Ceramic + 1 µF Tantalum or Ceramic). See *Figure 14* and *Figure 15* for decoupling examples.

For STM32F10xxx devices delivered in 100/144-pin packages, it is possible to improve the accuracy on low-voltage inputs by connecting a separate external ADC reference voltage input on V_{REF+} (refer to *Section 2.2.4*). The voltage on V_{REF+} may range from 2.4 V to V_{DDA}. If a separate, external reference voltage is applied on V_{REF+}, two 10 nF and 1 µF capacitors must be connected on this pin. In all cases, V_{REF+} must be kept between 2.4 V and V_{DDA}.

Figure 14. Power supply and reference decoupling for 100- and 144-pin packages

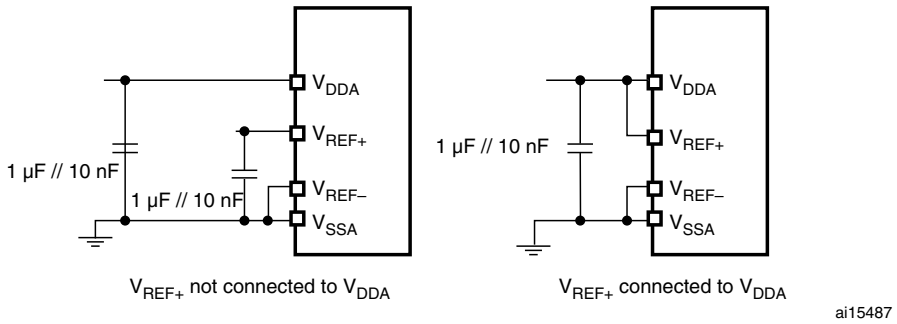
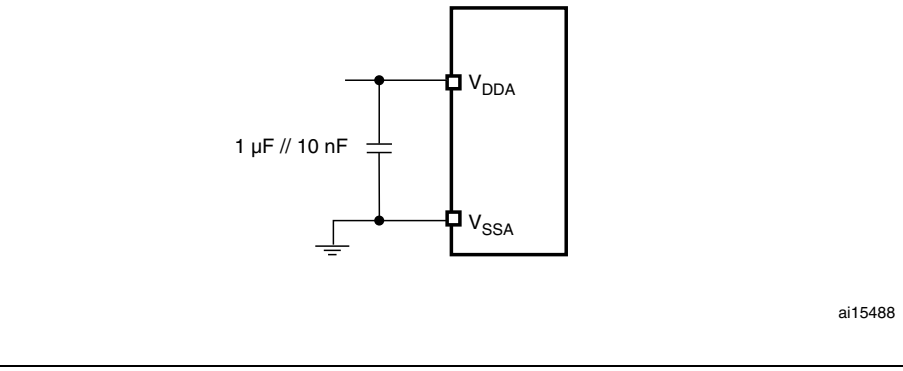


Figure 15. Power supply decoupling for 36-, 48- and 64-pin packages



2.2.2 Power-supply regulation recommendation

The power supply should have good line and load regulation since the ADC uses V_{REF+} or V_{DDA} as the analog reference and the digital value is the ratio of the analog input signal to this voltage reference. V_{REF+} must thus remain stable at different loads.

Whenever the load is increased by switching on a part of the circuit, the increase in current must not cause the voltage to decrease. If the voltage remains stable over a wide current range, the power supply has good load regulation.

For example: for the LD1086D2M33 voltage regulator, the line regulation is 0.035% typical when V_{IN} varies from 2.8 V to 16.5 V (when I_{load} = 10 mA), and the load regulation is 0.2% when I_{load} varies from 0 to 1.5 A (please refer to the LD1086 series datasheet for details).

The lower the line regulation value, the better the regulation. Similarly, the lower the load regulation value, the better the regulation and the stability of the voltage output.

It is also possible to use a reference voltage for V_{REF+}, for instance the LM236, which is a voltage reference diode of 2.5 V (refer to LM236 datasheet for more details).

2.2.3 Analog-input signal noise elimination

Averaging method

Averaging is a simple technique where you sample an analog input several times and take the average of the results by software. This technique is helpful to eliminate the effect of noise on the analog input in case of an analog voltage that does not change often.

The average has to be made on several readings that all correspond to the same analog input voltage. Make sure that the analog input remains at the same voltage during the time period when the conversions are done, otherwise you will add up digital values corresponding to different analog inputs, and you will introduce errors.

Adding an external filter

Adding an external RC filter eliminates the high frequency. An expensive filter is not needed to deal with a signal that has frequency components above the frequency range of interest. In this case, a relatively simple lowpass filter with a cutoff frequency f_C just above the frequency range of interest will suffice to limit noise and aliasing. A sampling rate consistent with the highest frequency of interest will suffice, typically 2 to 5 times f_C.

Note: The R and C that form the external filter should have values that match the conditions described in Section 2.2.5 and Section 2.2.6.

2.2.4 Matching the ADC dynamic range to the maximum signal amplitude

This method improves accuracy by a proper selection of the reference voltage or by using a preamplifier stage to obtain the maximum possible resolution using the full ADC output range.

Selecting a reference voltage (method for devices delivered in 100-/144-pin packages only)

The reference voltage is selected in the expected range of the signal to be measured. If the measured signal has an offset, then the reference voltage should also have a similar offset. If the measured signal has a defined maximum amplitude, then the reference voltage should

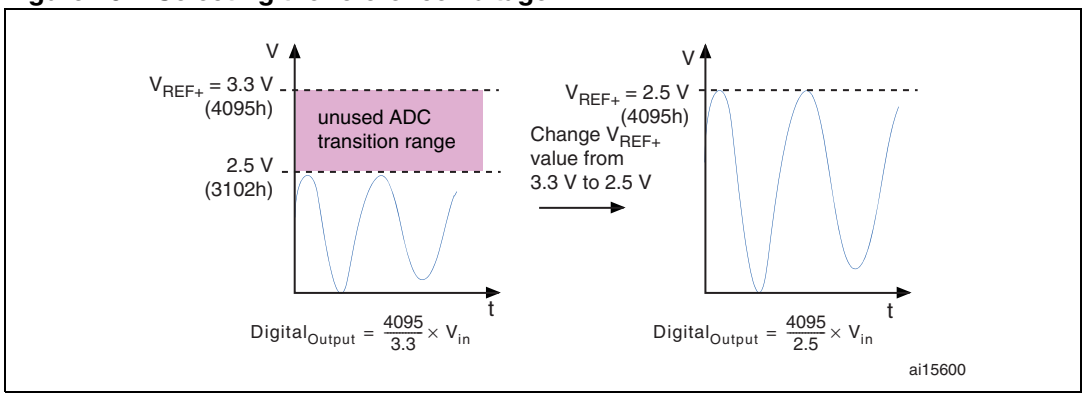
also have a similar maximum value. By matching this reference voltage to the measurement signal range, we obtain the maximum possible resolution using the full ADC output range.

In STM32F10xxx devices delivered in 100- and 144-pin packages, the ADC reference voltage is connected to the external V_{REF+} and V_{REF-} pins that should be tied to ground. This makes it possible to match the reference voltage and the measured signal range.

For example, if the measured signal varies between 0 V and 2.5 V, it is recommended to choose V_{REF+} = 2.5 V, possibly using a reference voltage like LM235 (see LM235 datasheet for more details). *Figure 16* illustrates these conditions.

Note: The voltage on V_{REF+} may range between 2.4 V and V_{DDA}.

Figure 16. Selecting the reference voltage



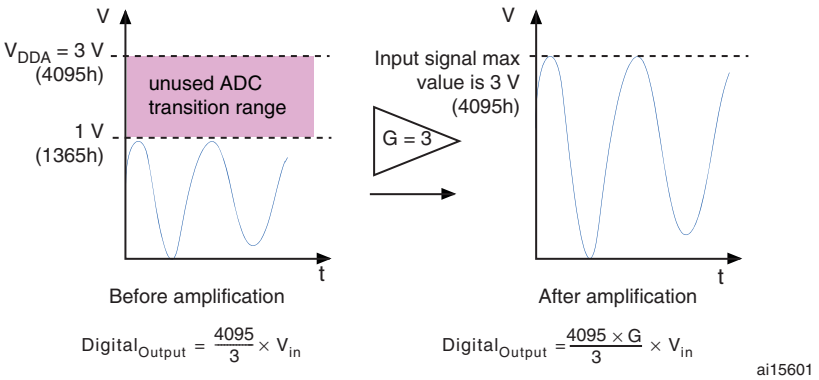
Using a preamplifier

If the measured signal is too small (in comparison with the ADC range) then it is good to use an external preamplifier. This method can be implemented with STM32F10xxx devices delivered in all packages, and more specifically so in packages that do not have the V_{REF+} input.

For example, if the measured signal varies between 0 V to 1 V and V_{DDA} is 3 V, the signal can be amplified so that its peak-to-peak amplitude is similar to the V_{DDA} value. The gain will then be equal to 3. *Figure 17* illustrates this example.

This amplifier can adapt the input signal range to the ADC range. It can also insert offsets between the input signal and the ADC input. Care must be taken in the preamplifier design not to generate additional errors (for example additional offset, amplifier gain stability, linearity, frequency response, etc.).

Figure 17. Preamplification



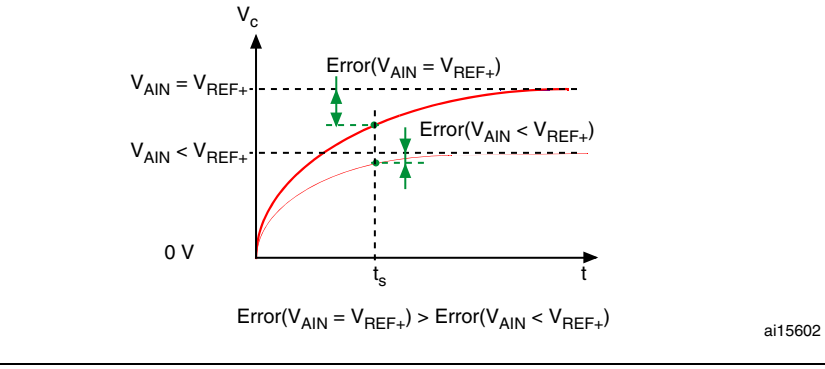
2.2.5 Analog source resistance calculation

Let us assume that the maximum error allowed is equal to 1/4 LSB. We will calculate the maximum source resistance allowed.

V_c is the voltage across the internal C_{ADC} capacitor (refer to *Figure 9*).

Then we have: $Error = V_{AIN} - V_c = \frac{1}{4}LSB$

Figure 18. Worst case error: $V_{AIN} = V_{REF+}$



Let t_s be the sampling time.

$t_s = T_S/f_{ADC}$, where T_s is the sampling time evaluated by cycles (1)

For a given t_s, the error corresponding to $V_{AIN} = V_{REF+}$ is greater than the error corresponding to $V_{AIN} < V_{REF+}$ because the C_{ADC} capacitor takes more time to charge from 0 V to V_{AIN} when $V_{AIN} = V_{REF+}$ than it takes when $V_{AIN} < V_{REF+}$ (refer to *Figure 18*). So $V_{AIN} = V_{REF+}$ is the worst case to be taken into account in the demonstration of the maximum source resistance.

$$Error = V_{REF+} - V_{REF+}\left(1 - e^{-\frac{t_s}{R_{max}C_{ADC}}}\right) = \frac{1}{4} \times \frac{V_{REF+}}{2^N}, \text{ where:}$$

- $R_{max} = (R_{AIN} + R_{ADC})max$ (2)
- N is the ADC resolution (in our case N = 12)

This gives: $e^{-\frac{t_s}{R_{max}C_{ADC}}} = \frac{1}{2^{N+2}}$. Thus: $R_{max} = \frac{t_s}{C_{ADC} \times \ln(2^{N+2})}$ (3)

By combining equations (1), (2) and (3), we obtain:

$$R_{AINmax} = \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADCmax}$$

So for T_s = 7.5, f_{ADC} = 14 MHz, C_{ADC} = 12 pF and R_{ADC}max = 1 kΩ, the maximum source resistance allowed for an error equal to 1/4 LSB is:

$$R_{AINmax} = \frac{7.5}{14 \times 10^{6} \times 12 \times 10^{-12} \times \ln(2^{12+2})} - 1\text{k}\Omega$$

That is:

R_{AINmax} = 3.6 kΩ

Note: The use of a follower amplifier can reduce the resistance of the source effect because of its high input impedance and its very low output impedance. It isolates R_{AIN} from R_{ADC}. However, the amplifier introduces an offset error that should be taken into account.

2.2.6 Source frequency condition vs. source and parasitic capacitors

The external capacitance will not allow the analog input voltage to be exactly the same as V_{AIN} if the capacitor is not fully charged by the analog source. If the analog input signal changes, then the analog signal frequency (F_{AIN}) should be such that the time period of this analog signal is at least: $10 \times R_{AIN} \times (C_{AIN} + C_p)$.

T_{AIN} = analog signal time period = $1/F_{AIN}$.

We have: $T_{AIN} \geq 10 \times R_{AIN} \times (C_{AIN} + C_P)$

Therefore: $F_{AIN} \leq \frac{1}{10 \times R_{AIN} \times (C_{AIN} + C_P)}$

For example:

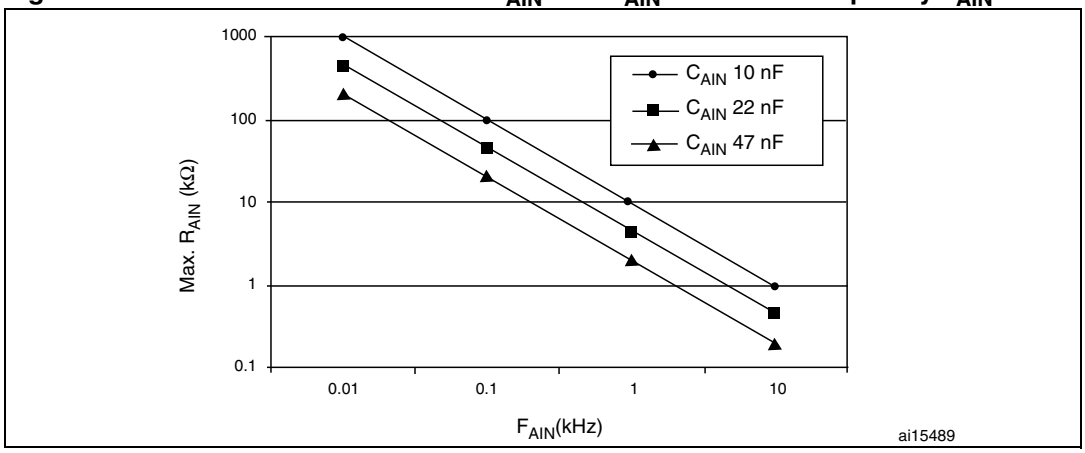
For R_{AIN} = 25 kΩ, C_{AIN} = 7 pF, C_p = 3 pF, this gives:

$$F_{AINmax} = \frac{1}{10 \times 25 \times 10^{3} \times (7+3) \times 10^{-12}}$$

Thus, the maximum frequency of the source will be: $F_{AINmax} = 400\ \text{kHz}$.

So for the above defined source characteristics (capacitance and resistance), the frequency of the source must not exceed 400 kHz, otherwise the ADC conversion result will be not accurate.

Figure 19. Recommended values for R_{AIN} and C_{AIN} vs. source frequency F_{AIN}



2.2.7 Temperature-effect compensation

One method would be to fully characterize the offset and gain drift and provide a lookup table in memory to correct measurement according to temperature change. This calibration involves additional cost and takes time.

The second method consists in recalibrating the ADC when the temperature change reaches given values, by using the internal temperature sensor and the ADC watchdog.

2.2.8 Minimizing Injection current

Check the application to verify whether any digital or analog input voltage can be less than V_{SS} or V_{SSA}. If it is the case, a negative injection current will flow from the pins. The effect on the accuracy will be greater if a digital input is close to the analog input being converted.

Negative current injection on any of the standard (non-robust) analog input pins should be avoided as this would significantly reduce the accuracy of the conversion being performed on another analog input.

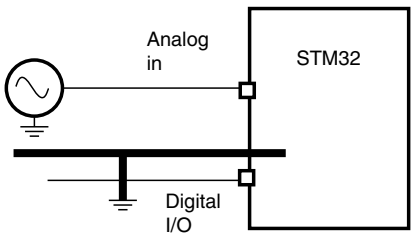
It is recommended to connect a Schottky diode between V_{SSA} and the I/O pin that can give birth to the negative injection current.

The ADC accuracy will not be affected by positive injection currents within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ (refer to the appropriate STM32F10xxx datasheet, I/O port characteristics section).

2.2.9 Minimizing I/O pin crosstalk

The noise produced by crosstalk can be reduced by shielding the analog signal by placing ground tracks across it. *Figure 20* shows the recommended grounding between signals.

Figure 20. Crosstalk between I/O pins



2.2.10 EMI-induced noise reduction

You can reduce EMI noise using proper shielding and layout techniques. The possible sources of emission must be physically separated from the receptors. They can be separated electrically by proper grounding and shielding.

Shielding technique

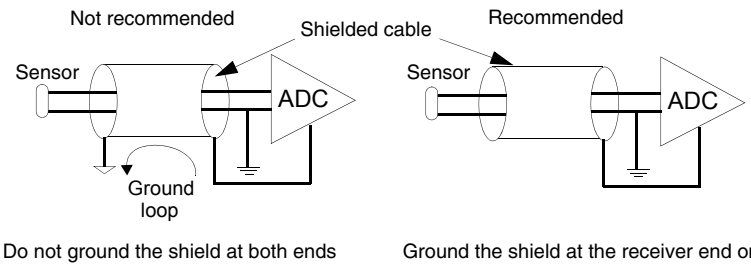
Placing ground tracks alongside sensitive analog signals provides shielding on the PCB. The other side of the two-layer PCB should also have a ground plane. This prevents interference and I/O crosstalk affecting the signal. See *Figure 21*.

Signals coming from distant locations (like sensors, etc.) should be connected to the PCB using shielded cable. Care should be taken to minimize the length of the paths of these types of signal on the PCB.

The shield should not be used to carry the ground reference from the sensor or analog source to the microcontroller. A separate wire should be used as ground. The shield should be grounded at only one place near the receiver such as the analog ground of the microcontroller. Grounding the shield at both ends (source and receiver) might lead to the creation of ground loops, with the result of current flowing through the shield. In this case, the shield acts like an antenna and the purpose of the shielding is lost.

The shielding concept also applies to grounding the chassis of the application if it is metallic. And it also helps remove EMI and EMC interference. In this case the mains earth ground is used to shield the chassis. Similarly DC ground can be used for shielding in case of the earth ground not being available.

Figure 21. Shielding technique



2.2.11 PCB layout recommendations

Separating the analog and digital layouts

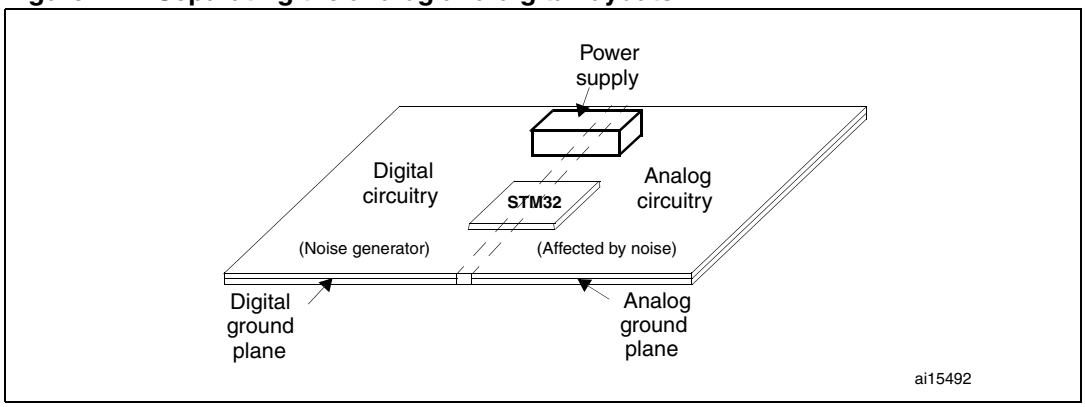
It is recommended to separate the analog and digital circuitry on the PCB (see *Figure 22*). This also avoids tracks crossing each other. The tracks carrying digital signals may introduce high-frequency noise in analog signals because of coupling.

The digital signals produce high-frequency noise because of fast switching.

Coupling of a capacitive nature is formed due to the metal connections (tracks) separated by the dielectric provided by the PCB base (glass, ceramic or plastic).

It is recommended to use different planes for analog and digital grounds. If there is a lot of analog circuitry then an analog ground plane is recommended. The analog ground must be placed below the analog circuitry.

Figure 22. Separating the analog and digital layouts



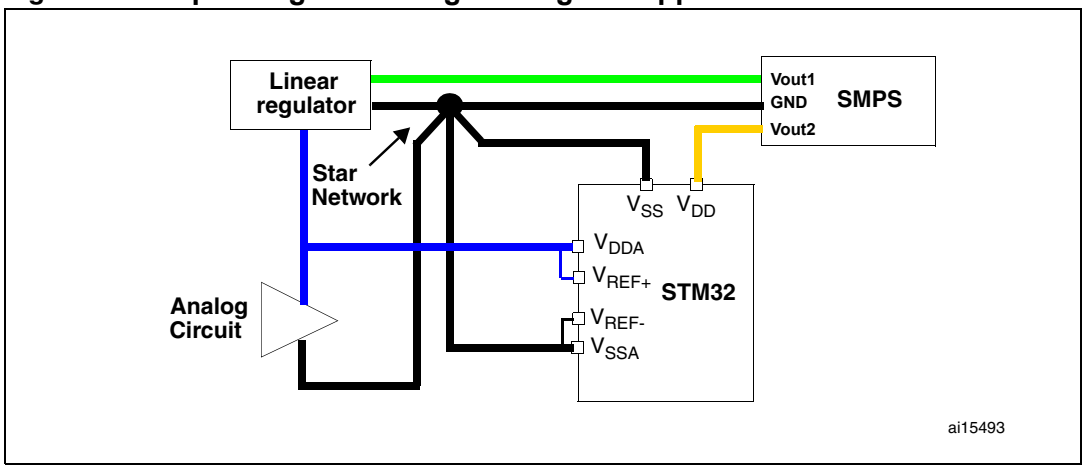
Separating the analog- and digital-circuit power supplies

It is desirable to have separate analog and digital power supplies in cases where there is a lot of analog and digital circuits external to the microcontroller (see *Figure 23*). Depending on the STM32F10xxx package, different analog and digital power supply and ground pins are available. The V_{DDA}/V_{REF+} and V_{DD} pins can be powered from separate power supplies.

If you use a switching-type power supply for the digital circuitry, you should use a separate linear supply for the analog circuit.

Also, if you expect a lot of noise on the DC power supply due to I/O switching etc., it is preferable to use a separate supply for the analog circuit.

Figure 23. Separating the analog and digital supplies



It is also recommended to connect the analog and digital grounds in a star network. This means that you must connect the analog and digital grounds at only one point. This prevents the introduction of noise in the analog power supply circuit due to digital signal switching. This also prevents current surges from affecting the analog circuit.

Using separate PCB layers for the supply and ground

- Two-layer PCBs

  For two-layer PCBs, it is recommended to provide a maximum ground plane area. The power supply (V_{DD}, V_{DDA}) should run through thick tracks. The two layers can have their ground shorted together via multiple connections in the overlap region if the two layers feature the same ground signals. The unused PCB area can be used as the ground plane.

  The other convention is to connect the unused PCB area on one layer to the positive supply (V_{DD}) and the unused area on the other layer, to ground. The advantage is a reduced inductance for power and ground signals. The maximum ground area provided for ground on the PCB results in a good shielding effect and reduces the electromagnetic induction susceptibility of the circuit.

- Multilayer PCBs

  Wherever possible, try to use multilayer PCBs and use separate layers on the PCB for power and ground. The V_{DD} and V_{SS} pins of the various ICs can be directly connected to the power planes, thus reducing the length of track needed to connect the supply and ground. Long tracks have a high inductive effect. The analog ground can be connected at one point to this ground plane. If so, it should be close to the power supply.

  A full ground plane provides good shielding and reduces the electromagnetic induction susceptibility of the circuit.

- Single-layer PCBs

  Single-layer PCBs are used to save cost. They can be used only in simple applications when the number of connections is very limited. It is recommended to fill the unused area with ground. Jumpers can be used to connect different parts of the PCB.

2.2.12 Component placement and routing

Place the components and route the signal traces on the PCB so as to shield the analog inputs.

Components like resistors and capacitors must be connected with very short leads. You can use surface-mounted device (SMD) resistors and capacitors. You can place SMD capacitors close to the microcontroller for decoupling purposes.

Use wide tracks for power, otherwise the series resistance of the tracks would cause a voltage drop. Indeed, narrow power tracks have a non-negligible finite resistance, so that high load currents through them would cause a voltage drop across them.

Quartz crystals must be surrounded by ground tracks/plane. The other side of the two-layer PCB below the crystal should preferably be covered by the ground plane. Most crystals have a metallic body that should be grounded. You should also place the crystal close to the microcontroller. You can use a surface-mounted crystal.

3 Conclusion

This application notes describes the main methods and application design rules to minimize STM32F10xxx ADC errors and obtain the best ADC accuracy.

The impedance and capacitance of the source to be converted as well as the PCB design are very important for the ADC application design, and so these parameters have to be taken into account.

Some methods depend on the application requirements and are a tradeoff between speed, accuracy and design topology.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
14-Nov-2008	1	Initial release.

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